U. - 16086

[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 1024 C

Unique Paper Code : 32341102

Name of the Paper : Computer System Architecture

Name of the Course : B.Sc. (H) Computer Science

Semester : I

Duration : 3 Hours Maximum Marks : 75

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Section A is compulsory.
3. Attempt any four questions from Section B.
4. Parts of a question must be answered together.

SECTION A

1. (a) Convert the hexadecimal number D5F2 to binary and octal number system. (2)

P.T.O.

(b) How can a D flip-flop be constructed using a JK flip-flop? Explain with the help of a block diagram. (2)

(c) How many 128×8 memory chips are needed to provide a memory capacity of 4096×16? (2)

(d) Represent the following decimal number 165.29 in BCD (2)

(e) What is Hardwired control unit? (2)

(f) Differentiate between Program Counter and Address Register. (2)

(g) Represent the number $(+12.5)_{10}$ as a floating point binary number with 16 bits. The normalized fraction mantissa has 9 bits, and the exponent has 7 bits. (3)

(h) Write micro-operations for implementing the following memory reference instructions :-

(i) BUN: Branch Unconditionally

(ii) ISZ: Increment and Skip if Zero (4)

(i) Construct a 32 X 1 multiplexer using eight 4 X 1 multiplexers and one 8 X 1 multiplexer. Give block diagram and explain its working by means of a function table. (4)

(j) Given the following Boolean function : (4)

$F = XY'Z + X'Y'Z + XYZ$

(i) Simplify F using Boolean algebra

(ii) Draw the logic diagram of the simplified Boolean expression

(k) What is Program Controlled I/O? What is Interrupt Driven I/O? Give one disadvantage of each. (4)

(l) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

(i) How many selection inputs are there in each multiplexer?

(ii) How many multiplexers are there in the bus? (4)

P.T.O.

4. (a) A Computer uses a memory unit with 32768 words of 24 bits each. Every binary instruction is stored in one word of memory. The instruction has four parts: two bits to specify mode, two bits to specify a processor register, an operation code and an address part.

(i) Draw the instruction word format and indicate the number of bits in each part.

(ii) How many addressing modes and number of operations are supported?

(iii) Specify the number of bits required in each of PC, AC and IR. (6)

(b) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline system for 100 tasks. What is the maximum speed up that can be achieved? (4)

5. (a) How is an interrupt processed in a computer? Explain with the help of interrupt cycle. (6)

(b) Using a general register computer with two address instructions, write a program to evaluate the arithmetic statement :

$$X = (C - D) * (E - F)$$ (4)

6. (a) The content of PC in the basic computer is 2AC (all numbers are in hexadecimal). The content of AC is 2EC3. The instruction format has three parts: mode, opcode and address. The content of memory at address 2AC is 832E. The content of memory at address 32E is 0821. The content of memory at address 821 is 8B9F. (Opcode 000 is for ADD operation, mode bit = 1 is for indirect addressing).

(i) Give block diagram of memory unit to give snapshot of the above representation and specify the instruction that will be executed.

(ii) Perform the binary operation in the AC when the instruction is executed. Also, specify the values of PC, AR, DR, AC and IR in hexadecimal at the end of the instruction cycle. (6)

P.T.O.

(b) Give block diagram of Direct Memory Access (DMA) controller. How does CPU initialize the DMA transfer? (4)